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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/690,402	10/20/2003	Billy Wayne Garrett JR.	9797-0141-999	5944

38426 7590 01/13/2005

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EXAMINER	
CHACE, CHRISTIAN	
ART UNIT	**PAPER NUMBER**
2187	

DATE MAILED: 01/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application N .	Applicant(s)	
	10/690,402	GARRETT ET AL.	
	Examiner	Art Unit	
	Christian P. Chace	2187	

-- The MAILING DATE f this communication appears n the c ver she t with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) *15-18* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/23/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☒ Other: *Requirement for Information*.

DETAILED ACTION

Election/Restrictions

Applicant's election of Group I in the reply filed on 15 July 2004 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Requirement for Information

Applicant and the assignee of this application are required under 37 CFR 1.105 to provide the following information that the examiner has determined is reasonably necessary to the examination of this application.

In response to this requirement, please provide a copy of each of the following items of art referred to in the specification (see paragraph 30):

Direct RDRAM™ 64/72-Mbit Data Sheet

Direct RAC Data Sheet

Direct RMC.d1 Data Sheet

A Logical View of the Direct Rambus Architecture

Direct Rambus Technology Overview

Direct Rambus Clock Generator Source Sheet

Direct Rambus RIMM™ Module Data Sheet

Direct Rambus Memory Controller Summary.

All of these are disclosed as 1998 documents.

The fee and certification requirements of 37 CFR 1.97 are waived for those documents submitted in reply to this requirement. This waiver extends only to those documents within the scope of this requirement under 37 CFR 1.105 that are included in the applicant's first complete communication responding to this requirement. Any supplemental replies subsequent to the first communication responding to this requirement and any information disclosures beyond the scope of this requirement under 37 CFR 1.105 are subject to the fee and certification requirements of 37 CFR 1.97.

The applicant is reminded that the reply to this requirement must be made with candor and good faith under 37 CFR 1.56. Where the applicant does not have or cannot readily obtain an item of required information, a statement that the item is unknown or cannot be readily obtained will be accepted as a complete reply to the requirement for that item.

This requirement is an attachment of the enclosed Office action. A complete reply to the enclosed Office action must include a complete reply to this requirement. The time period for reply to this requirement coincides with the time period for reply to the enclosed Office action.

Information Disclosure Statement

IDS submitted 20 October 2003 has been considered by examiner. A signed and initialed copy is attached hereto.

Specification

The disclosure is objected to because of the following informalities: In the first line of paragraph 1, application 09/457,155 has passed to issue and is not US Patent 6,708,248. In the first line of paragraph 5, "-bit" should be inserted after "64." In the second-to-last line of paragraph 92, application 09/395,160 has passed to issue and is now US Patent 6,370,668.

Appropriate correction is required.

Claim 1 is objected to because of the following informalities: A semicolon should replace the comma in line 7. Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-14 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

With respect to independent claims 1 and 11, the claims recite, "memory devices" in several places. It is unclear whether this is intended to be a plurality of memory devices. If so, it is recommended that applicants change the wording to "a plurality of memory devices" to avoid any confusion as to whether there are more than one being claimed.

The term "low bandwidth" in claims 1 and 11 is a relative term which renders the claim indefinite. The term "low bandwidth" is not defined by the claim, the specification

does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. The "memory devices" cannot be clearly or reasonable interpreted if examiner cannot ascertain the metes and bounds of the term "low bandwidth" which describes them.

The memory devices being individually incapable of communicating a first data block "with" the memory controller is not clear. First, what good is a memory device that is incapable of communicating? Does this mean that the memory device itself does not initiate the communication, but does supply the data when asked for it by a master? Or, does it mean a fault in that memory has been located, and it will not operate as a result? This is a significant distinction as examiner would need to search in class 714, for example, if there is any fault locating/responding. Second, what does "communicating a block with the memory controller," mean? Is this reads and writes from one to another, or do they both work together somehow to send and receive information with some other element?

Throughout claim 1, as well as claims 2 and 11, for example, use the phrase "configured to." This phrase does not make clear whether the referenced elements actually perform the actions modified by this phrase, and, can cast doubt on whether those claimed elements have patentable weight.

"At least a first plurality of memory devices" is claimed in line 7 of claim 1, for example. It is unclear whether this plurality is the same as the "memory devices" discussed supra, or a subset of them, or a completely different plurality of memory devices altogether.

"Communicate a first data block" is recited in line 9 of claim 1 as well as in claim 11. It is unclear whether this is a physical move of the memory chip, for example, or merely the data in the memory chip being transmitted/received.

With respect to claims 2 and 12, the claims recite, "the first plurality of memory devices is configured to "contribute" a second data block..." Again, it is unclear from the term "contribute" whether this is a physical allocation or a replacement algorithm implementation, for example. In addition, line 2 recites, "...less than the first data block," from which it is unclear what is less – is it less size, less data in it?

With respect to claims 3, 5, 7, and 9, the claims recite, "each one of the two channels [each channel] connecting a second plurality of memory devices to the memory controller." It is unclear whether the first channel has the first and second plurality of memory devices (in addition to the memory devices?) and the second channel also has the second plurality of memory devices. Or, does the first channel have the first plurality of memory devices, and the second channel have the second plurality of memory devices, respectively?

With respect to claim 13, the claim recites, "a first auxiliary channel." Is this the same element as, "the at least one auxiliary channel?" Or, is this a subset or distinct element?

Claims 4, 6, 8, and 14 depend upon the claims discussed supra and are rejected for at least the reasons set forth supra with respect to same.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-14 are rejected under 35 U.S.C. 102(b) as being anticipated by Farmwald et al (US Patent 5,243,703).

Examiner wishes to note that in light of the 35 USC 112, 2nd paragraph rejection discussed supra, examiner has applied the instant cited prior art of record in so far as the claims are clear.

With respect to independent claim 1, a memory system is disclosed in figure 9.

A memory controller connected to at least one channel is disclosed as a system or bus master, shown in figure 2, for example, as #11, with a CPU being a master being discussed in column 7, lines4-5. The at least one channel is the primary bus, #18, in figure 3. The primary bus is connected to the transceiver bus #65 of figure 9, which is included to interface multiple units to a higher order bus, as discussed in column 5, lines 39-41. An external bus being a higher order bus is disclosed in column 7, lines 45-50, for example.

Memory devices connected to the at least one channel is disclosed in figure 9, with #15-#17 being DRAMS, as discussed in column 23, line 1. One of the memory devices being individually incapable of communicating a first data block to/from the memory controller during a first time period is disclosed in column 8, lines 23-27 as a

failed memory block. If a device fails, it cannot transmit any data, and, therefore, is incapable of such transmission.

The memory controller communicating control information to at least a first plurality of the memory devices (the ones not "mapped out" as discussed in column 8, lines 23-27, e.g.) via the at least one first channel is disclosed in column 8, lines 38-50, which discusses accessing the "good" blocks of the memory devices.

The first plurality of memory devices being a multiplexed group on a channel is discussed in column 23, lines 52-53 and in column 24, lines 28-32. In addition, the bus being a multiplexed bus is disclosed in column 10, lines 33-35. By definition, those bus lines communicate data to and from the memory devices [that have not been mapped out due to failure]. This "first time period" is the specified time referred to in column 9, line 54, for example.

With respect to claims 2 and 12, column 8, lines 45-50 discuss mapping blocks according to addresses, with the block of a next address being "lower" than that of the first. "Lower" is interpreted to be "less than."

With respect to claims 3, 5, 7, 9, and 13, the at least one channel comprising 2, 4.5, 8, and 4 channels, respectively, is an inherent factor of design choice, as discussed in column 6, line 40, lines 62-63; column 7, lines 45-50, lines 55-57; column 12, lines 21-29, and column 21 and 22, under "Multiple Busses." Column 4, lines 60-65, explicitly discusses the nature of the choice being within the skill of one of ordinary skill in the art. Figure 9 shows a second plurality of memories connected to the second channel, with

each of Primary Busses #18 being a respective channel, with the memories attached thereto.

With respect to claims 4, 6, 8, 10, and 14, the number of memory devices *comprising* 16, 16, 8, 8, and 8 memory devices, respectively, is disclosed in column 21, lines 45-60.

With respect to independent claim 11, the claim appears to be very similar to independent claim 1, for which the similar elements will retain similar rejection in light of the applied prior art, with the following exception:

At least one repeater is disclosed in figure 9, #19 as a transceiver.

Conclusion

This Office action has an attached requirement for information under 37 CFR 1.105. A complete reply to this Office action must include a complete reply to the attached requirement for information. The time period for reply to the attached requirement coincides with the time period for reply to this Office action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christian P. Chace whose telephone number is 571.272.4190. The examiner can normally be reached on MAXI FLEX.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on 571.272.4201. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Christian P. Chace
Examiner
Art Unit 2187

DONALD SPARKS
SUPERVISORY PATENT EXAMINER

Donald Sparks
SPE, 2187